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Middle East Technical University

Department of Electrical and Electronics Engineering

# EE464: Static Power Conversion-II

# Hardware Project Final Report

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# Introduction

This is the final report for the hardware project of the EE464 Static Power Conversion II course prepared by Emine BOOSTancı group.

In this project an isolated DC/DC battery charger is designed according to the following specifications.

* Minimum Input Voltage: 20 V
* Maximum Input Voltage: 40 V
* Output Voltage: 12 V
* Output Power: 60 W
* Output Voltage Peak-to-Peak Ripple: 3%
* Line Regulation (Deviation of percent output voltage when input voltage is changed from its minimum to maximum or vice versa): 3%
* Load Regulation (Deviation of percent output voltage when the load current is changed from 10% to 100% or vice versa): 3%

Firstly, possible topologies are introduced to meet these requirements and the initial design considerations according to the selected design, flyback converter is presented. Then, the magnetic and controller design for this topology is presented. After that, simulation results for the circuit that can be physically realizable are given. Then the selected components are listed. Thermal analysis of the switching devices are also provided. After that experimental results of the designed circuitry are shared. Lastly, cost and compactness analysis of the circuit are presented in this report.

# Topology and Design Selection

For this project, the following isolated DC/DC converter topologies are assessed.

**Flyback Converter:**

Flyback converter topology is suitable for low to medium power applications (typically up to 100 Watts), which fits the 60W requirement.

Advantages:

* Flyback has the minimum number of components. There is only one transformer which is also used as an inductor.
* There is no restriction on the duty cycle.
* Design and control of the topology is the easiest.
* No need for resetting the core’s magnetic flux.

Disadvantages:

* Leakage inductance is a problem since it does not have a discharging path. Using snubbers decrease the efficiency of the converter. Adopting a two switch or interleaved topology will complicate the design and control of the converter.
* For high power topologies efficiency is the lowest compared to the other alternatives.
* Output voltage ripple is higher compared to other alternatives. Thus, additional filtering might be needed.

**Forward Converter:**

The forward converter is suitable for power levels from 50 Watts to a couple of hundred watts.

Advantages:

* This topology is generally more efficient than the flyback converter.
* This topology has better transient response compared to the flyback converter.
* This topology has better lower output ripple compared to the flyback converter due to the output inductor.
* This is the least complex topology after the flyback converter.
* There are no center tapped windings.

Disadvantages:

* This topology has a more complex magnetic design compared to flyback converter due to the additional inductor. Additional inductor will increase the magnetic and copper losses. Notice that the switching frequency seen by the inductor is twice of the switching frequency.
* Flux of the transformer must be reset in one switching cycle. Otherwise, the flux will aggregate and cause saturation which will result in problems in the power transfer. Therefore, the maximum duty cycle is limited. This will complicate the design and control of the converter. This will complicate the design of the converter.
* There are more components compared to the flyback converter thereby it is more expensive and less compact.

**Push Pull Converter:**

The push pull converter is suitable for medium power levels (100 Watts to a few kilowatts).,

Advantages

* Transformer size is reduced because the core is utilized more effectively.
* This topology has better lower output ripple and voltage regulation compared to the flyback and forward converter.
* A smaller variation in D can help achieve the desired output voltage with twice the gain compared to a forward converter.

Disadvantages:

* Two switches will have to be controlled with a phase shift of half a period. More difficult control. Deadtime adjustment may be required.
* Same problems with additional inductor are present too.
* Inductors’ core losses will happen at twice the frequency of operation.
* The duty cycle is also limited for this topology.
* This topology has more components than the flyback and forward converter.
* This topology is more complicated than the other two topologies.

**Half Bridge and Full Bridge Converter:**

The Half Bridge and Full Bridge Converters are suitable for medium to high power ranges (typically 100 Watts to over 500 Watts).

Advantages

* Same advantages as push-pull but better efficiency and power density.
* Furthermore, the fill factor challenge eased compared to a push-pull converter since there is a single primary.

Disadvantages

* Same disadvantages as push-pull but complexity of the converter is increased.
* For full bridge converter additional switches increase the losses.
* For half bridge converter nonidentical switches might cause problems in terms of voltage division.

Push-pull, half and full bridge converter topologies are overdesign for this project since the output power is 60W. Therefore, the real candidates are flyback and forward converter topologies. Since there is a limit on the duty cycle and risk of flux accumulation on the core, the design and control of the forward converter. Also, additional inductance and 3rd winding increase the complexity of the magnetic design. Although the flyback converter’s efficiency is inferior due to the snubber circuit for leakage inductance discharge, an optimization or an application note can be utilized to optimize the efficiency of the converter. Moreover, two switch flyback topology can be used. Although this will increase the complexity due to the drive of the high side switch it will enable us to feed the stored energy on the leakage inductor back to the input capacitor instead of dissipating it on the resistor in the snubber circuit. This will increase efficiency. Another disadvantage of the two switch flyback is the fact that the duty cycle is limited to 0.5 due to the diodes on the input side. For now, the snubber design will be selected as the solution of the discharge path of the leakage inductor. It is aimed to complete the first design as soon as possible so that the design can be changed to two switched flyback is efficiency would be smaller than the aimed one.

Another important decision is whether to operate at CCM or DCM. Since flux drops zero at DCM of operation the magnetic core is utilized better. Also, control of the converter is easier due to the linear relationship between output voltage and duty cycle as can be seen in Figure 1. However, the analytical understanding of the DCM operation is harder in terms of equations therefore the design is more complex. In addition to this, the current ripple is higher for DCM operation. This will increase semiconductor losses. Furthermore, the output voltage ripple will increase, and an additional filter might be used to meet the 3% voltage ripple condition. Since a controller that can operate at CCM is found, to meet voltage ripple and load regulation criteria CCM operation is chosen.

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Figure 1 Bode Plots For DCM and CCM Mode of Operation

After selecting the topology and the mode of operation, switching frequency, turns ratio and duty cycle range are determined.

* Switching frequency (fs) selection: Switching frequency is chosen as 100 kHz. Increasing the switching frequency will enable us to have a smaller ripple at the output and give us the chance to decrease Lm. Decreasing Lm will enable us to utilize the core more efficiently. However, increasing frequency will increase the switching losses of the transistors, core losses and conduction losses. In addition to these, increase in switching frequency will increase the leakage inductances. Therefore, an optimal choice is made as 100 kHz. Also, it is aimed to complete the project in PCB which will solve the leakage inductance problem compared to Pertinax.
* Turns Ratio (N) and Duty Cycle Range (D) Selection: The input output specifications shows that the voltage will be decreased. Hence, choosing duty cycle below 0.5 is more logical and will ease turns ratio selection. Also, selecting maximum duty cycle high will increase the effects of the parasitic inductances and resistances which will magnify the effect of the nonidealities to the input output relation. The voltage relationship for the flyback topology is given below. According to this equation, the maximum and minimum duty cycle for different turns ratio is plotted in Figure 2. The turns ratio is selected as 1 since the understanding will be much easier and the maximum and minimum duty cycles are computed as 0.375 and 0.23 which are smaller than 0.5.



Figure 2 Duty Cycle vs Turns Ratio wrt Max and Min Voltage Gain

# Magnetic Design

In this part, we need to decide the magnetizing inductance on the primary side , a magnetic core, number of turns and the winding cables. Then, the magnetic and copper losses of the transformer are calculated. Lastly, the transformer is wound and magnetizing and leakage inductances and primary and secondary winding resistances are measured by LCR meter.

Before selecting the core, the magnetizing inductance in the primary side is determined. The decided so that the converter does not work in DCM mode but also the peak inductor current is not too high so that the core is not saturated. For these conditions the average inductor current and the current ripple are important. The average inductor current depends on the average current and duty cycle. To find the average input current the efficiency of the converter must be known. For now, the efficiency of the converter will be estimated as 70%.

Input current is equal to the primary side inductor current for DTs and zero for the rest of the switching period. The relationship between the primary side inductor current and the input current is given as follows.

Maximum and minimum average primary side inductor current are calculated as 11.43 A and 9.29 A respectively.

For the current ripple Krf is defined as the ripple factor as given in Figure 3.

A diagram of a line graph

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Figure 3 Ripple Factor

In order to avoid DCM operation KRF must be smaller than 1. Also, smaller KRF will decrease the output voltage ripple. However, lower KRF might increase the transformer flux which will lead to the saturation of the core. For safety 0.5 KRF is avoided. The needed inductance can be calculated as follows.

Primary side inductance is selected as 20 µH.

The saturation must be avoided to transfer power efficiently. The saturation is determined by the peak current. The primary peak current is plotted with respect to the input voltage in Figure 4.



Figure 4 Peak Primary Current vs Input Voltage

From Figure 4 it can be seen that the maximum peak current occurs when the input voltage is minimum. This value is calculated as 13.3 A.

Now it is time for magnetic core selection. For core selection there are two options, a distributed gap core or a ferrite core. The relative permeability of the distributed gap cores is small, the leakage inductance is higher with respect to the ferrite core. Since the leakage inductance is dangerous for the switches a ferrite core 0R45530EC which is available in the laboratory is selected. One of the reasons to select this core is that its cross section area is high thus the saturation of the core can be easily avoided. Also, operating around 100 mT is aimed so that the core losses will be minimized although the volume of the core is increased. Another reason for selecting this core is the fact that its window area is the largest. This will ease the winding procedure.

To decide the number of turns in the primary side the core flux density and the length of the air gap will be considered. Half of the flux passing through the center leg of the core will be passing through the side legs. Nevertheless, the cross section area of the side legs is not exactly half of the cross section area of the center leg. Therefore, the magnetic field density will not be equal in the center leg and the side legs. It is known that the maximum primary current will occur when the duty cycle is maximum. Thus, the maximum magnetic field density will occur in the maximum duty cycle. The relationship between primary turns number and magnetic field density is given below.

To illustrate the relation between magnetic flux density and primary turns number these two are plotted with respect to each other in Figure 5. It can be seen that the center leg saturates more than the side legs.



Figure 5 Magnetic Field Density vs Primary Turns Number

Before selecting the primary turns number, we need to also consider the air gap length. Since the relative permeability of the core is 2300 the reluctance of the core is negligible with respect to air gap reluctance. The magnetic circuit of the transformer is given in Figure 6. Reluctance of the side legs and center leg can be found as follows.

A diagram of a circuit

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Figure 6 Magnetic Circuit of the Transformer

In order to determine the primary turns number, the air gap length is plotted with respect to the primary turns number in Figure 7.

From Figure 5 it can be seen that increasing the primary turns number will decrease the magnetic field density. However, increasing the primary turns number will also increase the air gap length. This is not desired due to the increasing fringing fields with increasing airgap length which can be seen from Figure 7. From both of these figures, the primary turns number is selected as 6. It can be seen that maximum magnetic flux density of the center leg is 1.05 T and air gap length is 5 mm for the selected turns number. The peak magnetic flux density is small enough to minimize the core loss and also the air gap length is small enough to ignore the fringing fields.

Magnetic field density vs the duty cycle for center and side legs are given in Figure 8.



Figure 7 Air Gap Length vs Primary Turns Number



Figure 8 Field vs Duty Cycle

Now we need to choose an AWG cable for primary and secondary. First, the skin depth is calculated for the switching frequency which is 100 kHz.

The copper area must be equal or smaller than the strand area. A litz wire found in the laboratory with AWG 28 is used whose strand section is 0.08 mm2.

Now we need to find how many cables to parallel in order to carry primary and secondary currents. Thereby, the rms value of the primary and the secondary currents are calculated. RMS value for an inductor current given in Figure 9 can be calculated as follows.

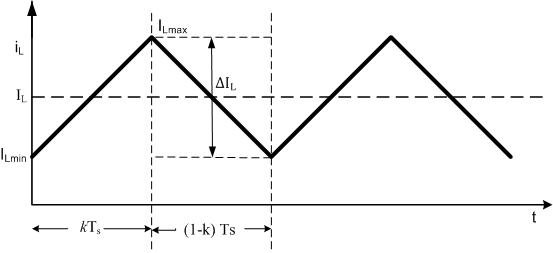


Figure 9 Typical Inductor Current

According to this formulation rms primary current vs input voltage is plotted in Figure 10. From Figure 10 it can be seen that the rms primary and secondary currents reach their maximum value of 11.5 A at minimum input voltage.



Figure 10 RMS Primary Current vs Input Voltage

The current density is chosen as 3.5 A/mm2.

For primary and secondary the number of parallel cables is calculated as 41. There are more than 50 parallels in the litz wire found in the laboratory. Since the total number of wires cannot be counted for fill factor calculation it is taken as 70 and for loss calculation it will be taken as 50. Henceforth, worst case scnerio will be assessed. The area of an AWG28 cable is 0.08 mm2. Total cable area can be calculated as follows.

The window area of the core is calculated from its dimensions as 375 mm2.

The fill factor is acceptable up to 0.3 to 0.4. Although our choice might seem like an overdesign, increasing the fill factor will complicate the wounding process. Thereby, the leakage inductance might be increased due to a poor wounding process.

Since the radius of the conductor is chosen smaller than the skin depth both AC resistance is quite the same as the DC resistance. This is verified by a website that measures the AC resistance of a specified cable [1]. The mean length turn of the core is calculated from the geometry in order to find the length of the wounded cable. Also, a safety factor of 1.5 is taken due to the cable thickness. This mean length turn is multiplied by the turns number to find the total length of the cables.

Maximum copper losses can be calculated from the maximum rms current which is found as 11.5 A for primary and secondary.

For core losses an excel file is obtained for ferrite materials from [2]. In this Excel file, Steinmetz coefficients are available. Steinmetz equation and coefficients for the R type material are given below.

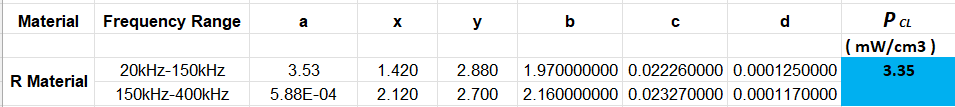


Figure 11 Steinmetz Coefficients for R Material

For maximum core loss, the maximum peak to peak ripple flux density which is 0.036 mT has been chosen. For operating temperature and frequency, 60°C and 100kHz are chosen respectively. Core loss density is calculated as 3.35 mW/cm3 for this operation condition. To find the core loss the core loss density is multiplied by twice the volume of the core (volume of the core is 208 cm3). Since two EC cores are used. Total core loss is found to be 0.364 WSince we operate at high frequencies this is expected. In order to use in unideal modelling of the converter Rcore can be found as follows.

After wounding the transformer LCR meter is used to calculate the leakage and magnetizing inductance. Since the LCR meter is not reliable for resistance calculations, to calculate the resistance windings are connected to the power supply and the maximum current is set to 5A. Then the voltage across the windings is measured by the multimeter and resistance is calculated from the Ohms Law. Supplied voltage is not used since the resistance of the cables that are used to connect the power supply and transformer is comparable with the winding resistance. For both windings voltage is measured as 0.023 V when 5A is supplied by the DC power supply. This means the resistance of the primary and secondary windings is 4.6 mΩ which is close to our calculations.

To understand the logic of the measurement technique of the leakage and magnetizing inductance equivalent model of the transformer given in Figure 12 is investigated. First, the secondary side is left open circuited. The measurement gives us the sum of primary leakage inductance and magnetizing inductance. Nevertheless, the measurement can be taken as magnetizing inductance since leakage inductance is much smaller than the magnetizing inductance. Magnetizing inductance is measured as 21.97 µH. For leakage inductance calculation, the secondary is kept short circuited, and inductance is measured. This measurement corresponds to primary leakage inductance plus secondary leakage paralleled magnetizing inductance. Since leakage inductance is much smaller than the magnetizing inductance, secondary leakage paralleled magnetizing inductance can be approximated as secondary leakage inductance. Thus, measured inductance 0.24 µH is the sum of primary and secondary leakage inductances. Since the turns ratio is 1, we can assume that leakage inductances are equal. This will yield primary and secondary leakage to be 0.12 µH. Measurements for open and short circuited secondary are given in Figure 13 and 14 respectively.

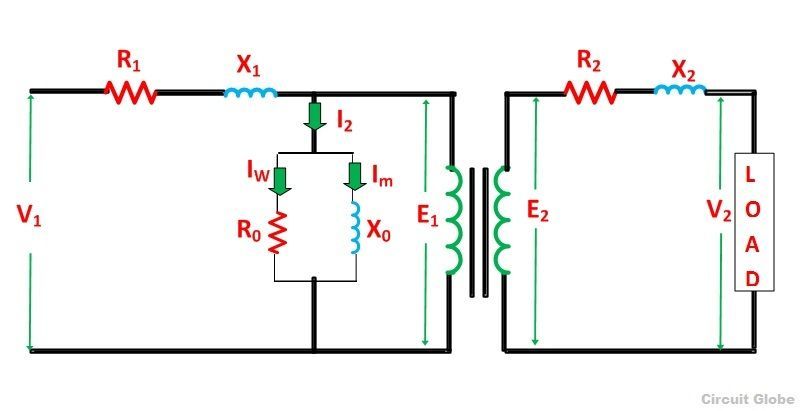


Figure 12 Equivalent Circuit of the Transformer

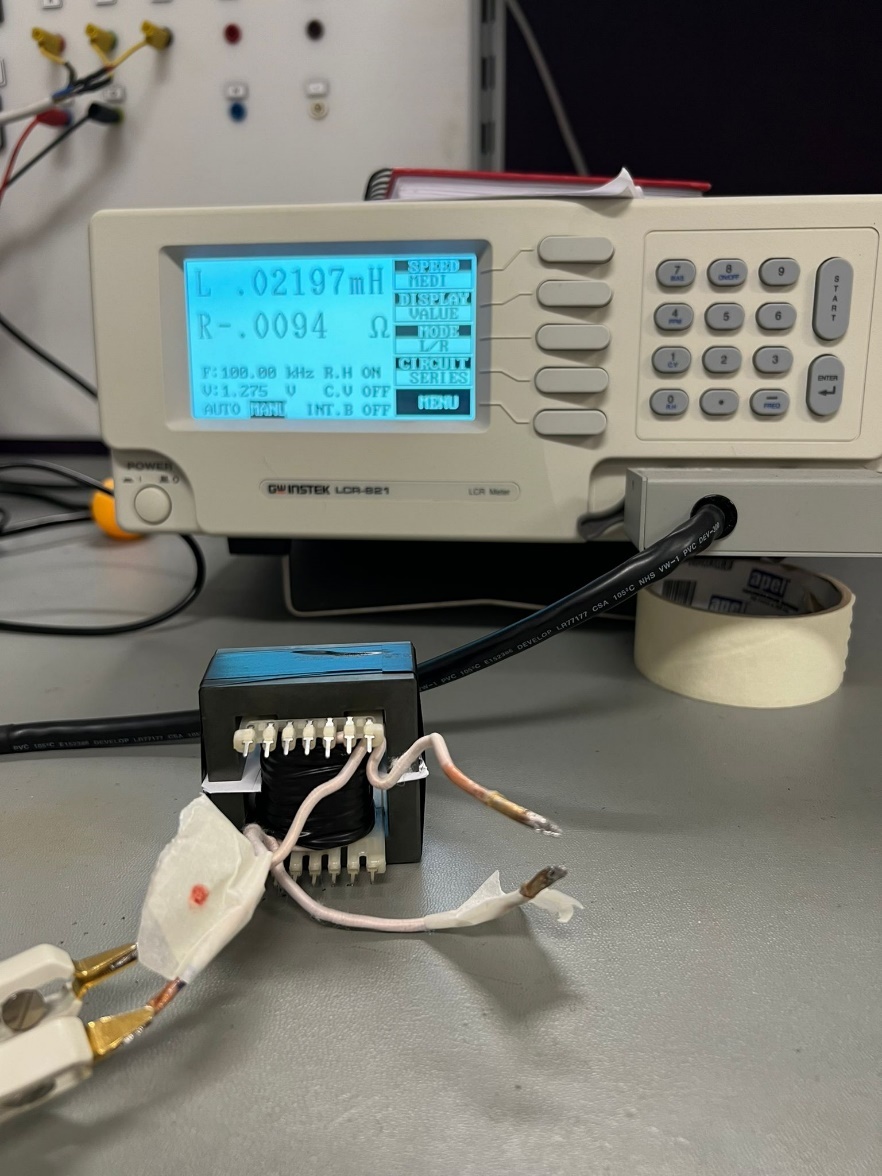


Figure 13 Open Circuit Measurements

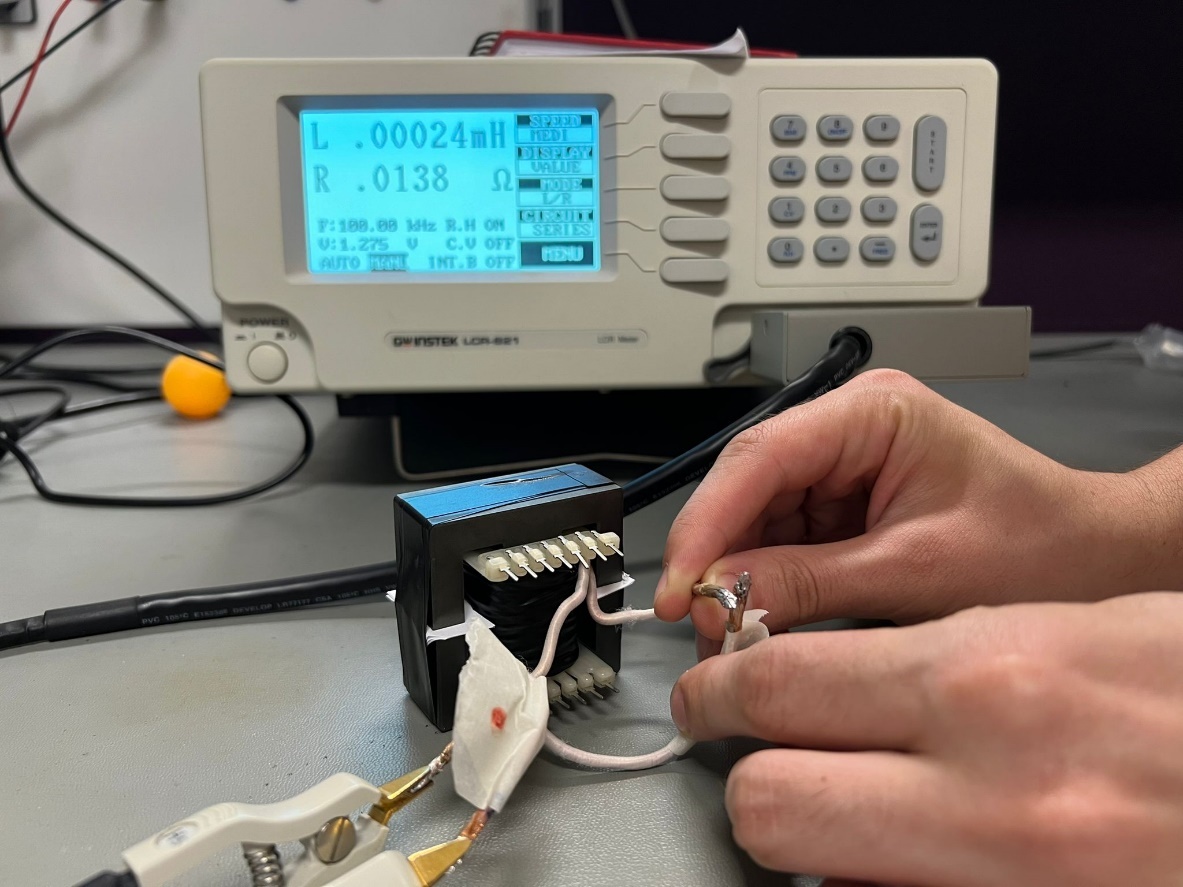


Figure 14 Short Circuit Measurements

# Controller Design

UC3843 is selected for output voltage control since it is commonly used for voltage control of DC/DC converters. UC3843 has peak current and voltage control features which are both used at our design. Moreover, UC3843 can provide up to full duty. For simulations LTSpice counterpart of the UC3843 which is LT1243, is used. The basic schematic of the controller network is given in Figure 15.

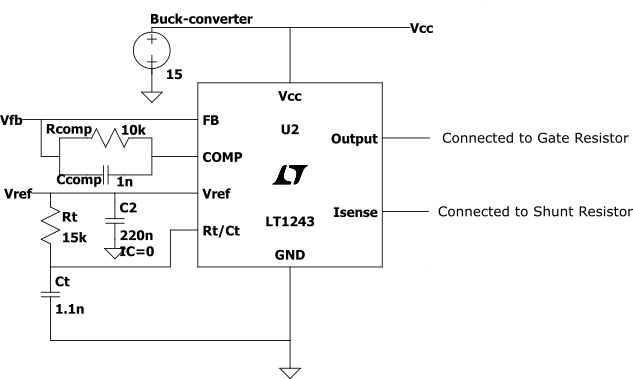


Figure 15 Controller Network

According to the datasheet of UC3843 [3] supply voltage of the controller must be between 8V to 30V. Since input voltage is between 20V to 40V the input cannot be directly used to feed it. Hence, a controlled buck converter with 10V to 40V rated input capability is used for this purpose. The controller gives gate signals at the output pin and 5V output at Vref terminal. The remaining parts of the controller are explained below.

**Rt/Ct Oscillator:** Rt/Ct oscillatorgenerates the sawtooth signal that is used for generating the switching signal. Frequency of the Rt/Ct oscillator sets the CCM mode switching frequency. The formula for the Rt/Ct oscillator frequency is as follows:

Rt and Ct are chosen 15 kΩ and 1.1 nF respectively. This will yield switching frequency to be equal to 104 kHz.

**Voltage Feedback Network:** Controller sets the duty of the gate signals according to the voltage error generated by the internal error amplifier. This error amplifier is a basic subtracter designed with an op amp whose inputs are internally generated 2.5V and voltage at Vfb pin. To set output voltage optocoupler network given in Figure 16 is used.

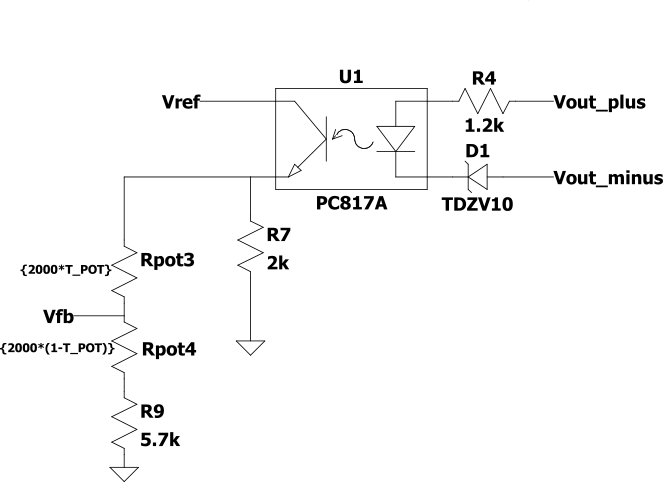


Figure 16 Optocoupler Network

The current transfer ratio of the PC817A optocoupler is very close to 1. Furhermore, resistance of the branch with potentiometer is relatively higher than 2 kΩ. Therefore, it can be assumed that current on the 2 kΩ branch is same as the 1.2 kΩ resistor. The branch with potentiometer enables us to set the output voltage reference to a value between 12.2 V to 13.1 Volt.

At steady state average voltage of the Vfb must be 2.5 Volts so that the output of the error amplifier will be zero and keep the duty constant. Tpot indicates the percentage of the potentiometer. According to this definition voltage and current of the 2 kΩ resistor can be found as follows.

The voltage on the 1.2 kΩ resistor can be expressed as follows.

The output voltage can be expressed as follows.

From the output voltage expression it can be seen that output voltage can be set to the desired value with potentiometer. The zener diode is used to apply full duty until output voltage reaches 11V which will increase the transient speed of the converter.

**Compensator:** 10 kΩ resistance and 1 nF capacitor are paralelled between Vref and Compensator pins of the UC3843 as shown in Figure 15. This adds a zero to the system which increase the phase margin and advance transient response.

**Peak Current Conrtol:** UC3843 controller has a current sense pin to limit the maximum switch current. Limiting the maximum switch current, which is also the transformer current, will enable to set the maximum power that will be transferred to the secondary. Also, it can be used for safety and preventing core saturation. UC3843 cuts the PWM output when the voltage of the current sense pin is 1V. Therefore, the sense resistor placed under the switch must be selected so that it will have 1V voltage drop when limiting current pass through it. In the magnetic design section the maximum primary transformer current is determined as 13.3 A. However, parasitic resistors series with the sense resistor will change the current sense pin since the resistance of the sense resistor is quite low. In addition to this the efficiency is approximated as 70% in magnetic design section. If the resultant efficiency is lower than the anticipated efficiency, the core will not be able to transfer the rated power. Therefore, the maximum current is chosen as 18A. The selected mosfet can carry 35A at 100 °C and the core remains unsaturated at 18 A (0.18 T). 18 A will result in 1V drop for 55mΩ. For sense resistor four 15 mΩ resistors are connected in series.

# Simulation Results

The circuit that is simulated in LTspice can be found in Fig. 17.

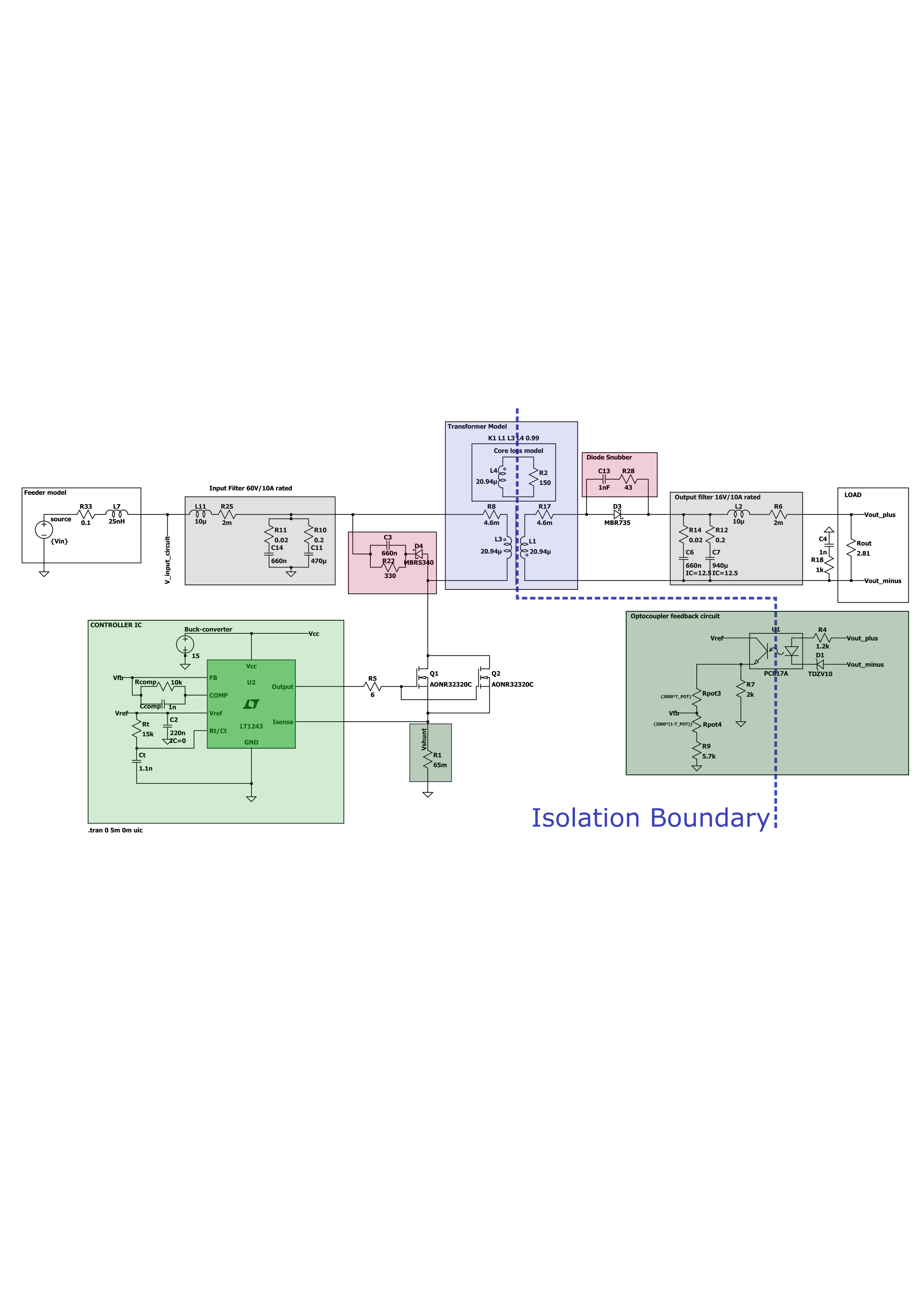


Figure 17 Simulated Circuit

The simulation was conducted using input voltages of 20, 25, 30, 35, and 40 volts, along with a set output voltage reference of 13V. The results show that our circuit achieves an efficiency of approximately 75-80% when implemented practically. The distribution of the input power averaging all results is shown in Fig 18. Detailed simulation results are shown in the Table X.

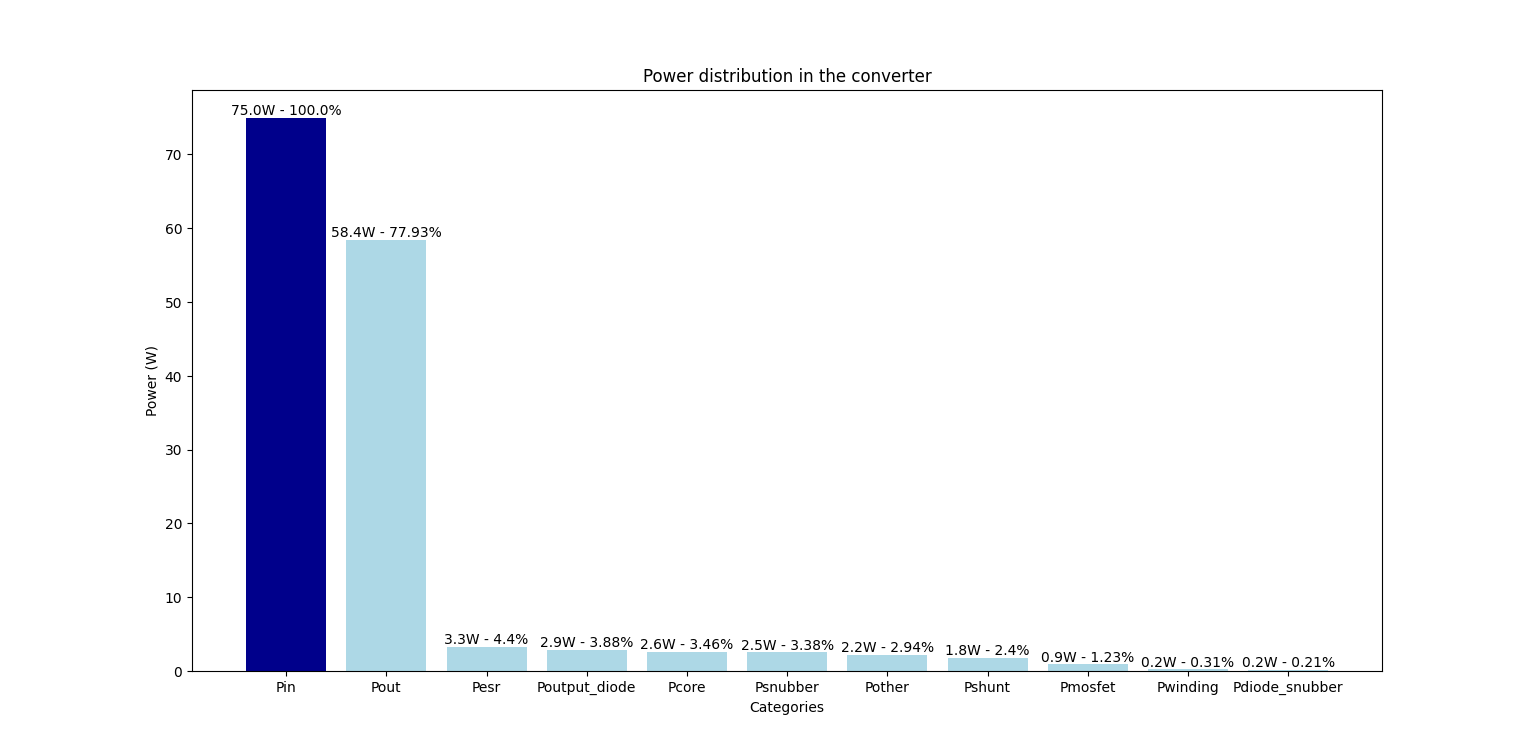


Figure 18 Power distribution in the converter

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Vin | Vset | Efficiency | **Duty** | **Iin-mean** | **Iout-mean** | **Pin(w)** | **Pout(w)** | **Psnubber** | **Pdiode\_snubber** | **Pmosfet** | **Pcore** | **Pwinding** | **Psnubber\_diode** | **Vds** | **Vout\_ripple** | **pdiode\_rect** | **Pshunt** | **Pesr** |
| 20.0 | 13.0 | 71.2 | 46.0 | 3.9 | 4.6 | 80.2 | 57.1 | 3.0 | 0.1 | 0.9 | 1.7 | 0.3 | 0.6 | 53.0 | 0.5 | 3.0 | 2.2 | 5.3 |
| 25.0 | 13.0 | 77.6 | 41.0 | 3.0 | 4.6 | 74.8 | 58.1 | 2.6 | 0.1 | 0.9 | 2.2 | 0.3 | 0.6 | 56.0 | 0.4 | 2.9 | 1.6 | 4.2 |
| 30.0 | 13.0 | 80.1 | 35.0 | 2.4 | 4.6 | 73.6 | 59.0 | 2.5 | 0.2 | 0.9 | 2.6 | 0.2 | 0.5 | 60.0 | 0.4 | 2.9 | 1.2 | 3.5 |
| 35.0 | 13.0 | 80.5 | 31.0 | 2.1 | 4.6 | 73.2 | 59.0 | 2.3 | 0.2 | 0.9 | 3.0 | 0.2 | 0.5 | 63.8 | 0.4 | 2.9 | 3.0 | 1.0 |
| 40.0 | 13.0 | 80.8 | 28.0 | 1.8 | 4.6 | 73.0 | 59.0 | 2.3 | 0.2 | 1.0 | 3.5 | 0.3 | 0.4 | 68.0 | 0.3 | 2.8 | 0.8 | 2.7 |
| Mean Values | | **78.06** | NA | **2.64** | **4.58** | **74.95** | **58.41** | **2.53** | **0.16** | **0.92** | **2.59** | **0.23** | **0.52** | **60.15** | **0.40** | **2.91** | **1.8** | **3.3** |

**References**

[1] W. (n.d.). Round Wire ac Resistance Calculator. <https://chemandy.com/calculators/round-wire-ac-resistance-calculator.htm>

[2]“Magnetics - Ferrite Core Loss Calculator.” <https://www.mag-inc.com/Design/Design-Tools/Ferrite-Core-Loss-Calculator>

[3] Texas Instruments. (2022). \*UCx84x Current-Mode PWM Controllers\* (Rev. G). Retrieved from <https://www.ti.com/lit/pdf/SLUS223>